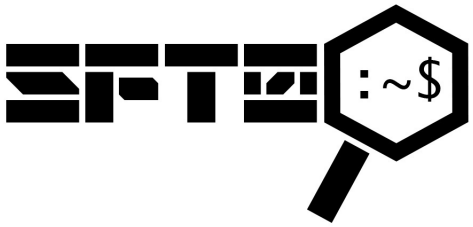

The "SFT0 CPU" 8bit RISC microprocessor

Archer Computer Inc

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1 Introduction

This Manual describes the assembly language format, and how to write assembly language programs for the "SFT0 CPU" microprocessor. Detailed information on the operation of specific assemblers is available in the Operator's Manual and Installation Guide for each specific assembler.

2 Computer Organization

2.1 Working Registers

The "SFT0 CPU" provides the programmer with three 8-bit "scratchpad" registers. These three working registers are numbered and referenced via the integers 0, 1, 2; by convention, these registers may also be accessed via the letters A, B, and C respectively.

Microprocessor also has a special register PC (Program Counter), which is a 16bit register used to point the address in RAM for the current instruction that microprocessor needs to execute.

In addition to the three 8-bit registers, the microprocessor also has 1-bit Flag Register, which is not accessed directly.

2.2 Memory

The programmer visualizes memory as a sequence of bytes, each of which may store 8 bits (represented by two hexadecimal digits). The bits stored in a memory may represent the encoded form of an instruction or may be data. The address space is being between 0x0000 and 0xFFFF included.

3 Standard "SFT0 CPU" Instructions

Every instruction has fixed size of 32bits (4 bytes) and encoded in "Big Endian" format.
Terminology:
Rx - Any general purpose register (0, 1, or 2).
KK - Any 8bit value.
KKKK - Any 16bit value.

3.1 ADD Rx, KK

Description: This instruction adds the value KK to the value of register Rx, then stores the result in Rx.

Mnemonic	Opcode
ADD Rx, KK	00 0x 00 KK

3.2 XOR Rx, KK

Description: This instruction performs a bitwise exclusive OR on the value KK and the register Rx, then stores the result in Rx.

Mnemonic	Opcode
XOR Rx, KK	01 0x 00 KK

3.3 AND Rx, KK

Description: This instruction performs a bitwise AND on the value KK and the register Rx, then stores the result in Rx.

Mnemonic	Opcode
AND Rx, KK	02 0x 00 KK

3.4 OR Rx, KK

Description: This instruction performs a bitwise OR on the value KK and the register Rx, then stores the result in Rx.

Mnemonic	Opcode
OR Rx, KK	03 0x 00 KK

3.5 LD Rx, KK

Description: This instruction loads the value KK into the register Rx.

Mnemonic	Opcode
LD Rx, KK	04 0x 00 KK

3.6 MOV Rx, Ry

Description: This instruction copies the value of register Ry into the register Rx.

Mnemonic	Opcode
MOV Rx, Ry	05 0x 00 0y

3.7 LDR Rx, KK

Description: This instruction loads 8bit from memory location KKKK into the register Rx.

Mnemonic	Opcode
LDR Rx, KKKK	06 0x KK KK

3.8 LDR Rx

Description: This instruction loads 8bit value from memory location specified by registers B and C into the register Rx. Register B hold upper 8bit memory location value while register C holds the 8 bottom bits.

Mnemonic	Opcode
LDR Rx	07 0x 00 00

3.9 STR Rx, KKKK

Description: This instruction stores 8bit value from the register Rx into the memory location KKKK.

Mnemonic	Opcode
STR Rx, KKKK	08 0x KK KK

3.10 STR Rx

Description: This instruction stores 8bit value from the register Rx to memory location specified by registers B and C. Register B hold upper 8bit memory location value while register C the bottom part.

Mnemonic	Opcode
STR Rx	09 0x 00 00

3.11 PUT Rx

Description: This instruction sends the value of the register Rx to Serial Out.

Mnemonic	Opcode
PUT Rx	0A 0x 00 00

3.12 JMP KKKK

Description: This instruction sets the Program Counter to the memory location KKKK.

Mnemonic	Opcode
JMP KKKK	0B 00 KK KK

3.13 JNZ KKKK

Description: This instruction compares the Flag Register to 0 and if equal, sets the Program Counter to the memory location KKKK.

Mnemonic	Opcode
JNZ KKKK	0C 00 KK KK

3.14 JZ KKKK

Description: This instruction compares the Flag Register to 1 and if equal, sets the Program Counter to the memory location KKKK.

Mnemonic	Opcode
JZ KKKK	0D 0x KK KK

3.15 CMPEQ Rx, KK

Description: This instruction compares the register Rx to the value KK and if equal, sets the Flag Register to 1, otherwise clears Flag Register.

Mnemonic	Opcode
CMPEQ Rx, KK	0E 0x 00 KK

3.16 HLT

Description: This instruction halts the processor.

Mnemonic	Opcode
HLT	44 44 44 44

3.17 NOP

Description: No operation.

Mnemonic	Opcode
NOP	33 33 33 33

4 Boot Process

The "SFT0 CPU" loads its rom at memory address 0x0000, then the PC is set to 0x1000 and execution begins.